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CasCaded Multilevel Inverter With Selective Harmonic Elimination-PWM Technique For Statcom Applications

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Abstract-This project presents a simple STATCOM using a cascaded multilevel inverter with the selective harmonic elimination pulse width Modulation (SHE-PWM) technique. DC link voltage balance is one of the major issues in a cascaded inverter based STATCOM and the most dominate harmonics in the system is lower order harmonics which affects the system performance. The proposed system is a simple STATCOM with selective harmonic elimination technique, by which the regulation of dc link voltages of inverters at reactive power compensation. The selective harmonic elimination techniques are also used to eliminate the most dominate harmonic in the system selectively. A new technique for getting an effective multilevel SHE-PWM control techniques is used to reduce lower order harmonics. The proposed modulation method also shows an feature of fixed switching angles across the entire range of the modulation index. The performance of the system is analysed by using MATLAB/Simulink and the experimental results have been verified.

Keywords— MATLAB Simulink, SHE-PWM control techniques, Multilevel Inverter, (STATCOM)

INTRODUCTION

The cascaded H-bridge multilevel inverters (CHMI) have been an attractive topology for STATCOM systems due to their modularization, extensibility and simpler control. They are formed by several series connected H-bridge inverters with separate DC sources or capacitors connected at each DC bus Depending on the modulation method and the number of levels in the output voltage waveform, near sinusoidal voltage output can be synthesized with relatively low switching frequencies. Several modulation and control techniques have been reported in the literature including carrier-based PWM, multilevel space vector modulation, stair case modulation and SHE-PWM. Other approaches have also been reported including one where multilevel SHE-PWM defined by the well-known multicarrier phase-shifted PWM (MPS-PWM) and another was based on single carrier sinusoidal PWM-equivalent SHE for a five-level waveform. A new variation of the problem was recently reported in where the DC voltage levels were made variables increasing the degrees of freedom in the formulation of the problem hence the number of harmonics to be eliminated without changing the physical structure of the converter. Several control strategies of CHMI based STATCOM systems have been implemented for Var/harmonic compensation and voltage regulation by using either frequency or time domain approaches to meet performance requirements. The objective of this work is to utilize the benefits of the new formulation of SHE-PWM multilevel control technique proposed in to STATCOM systems. A seven level cascaded H bridge converter is considered in this work. The target in this case is to find the optimal switching angles and the optimized levels of the dc voltages sources that eliminate nine non triple low order harmonics while controlling the fundamental component at a specific value. Selective harmonic elimination (SHE) is normally a two-step digital process. First, the switching angles are calculated offline, for several depths of modulation, by solving many nonlinear equations simultaneously. Second, these angles are stored in a look up table to be read in real time. This proposed an alternative real-time selective harmonic elimination (SHE) method based on modulation. A modified triangle carrier is identified that is compared to an ordinary sine wave. In place of the conventional offline solution of switching angles, the process simplifies to generation and comparison of the carrier and sine modulation, which can be done in minimal time without convergence or precision concerns. Static VAR compensation by cascading conventional multilevel inverters is an attractive solution for high-power applications. The topology consists of standard multilevel inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of

the inverters, the number of levels in the output voltage waveform can be increased.

II PROPOSED MULTILEVEL INVERTER

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels.

This proposed converter consists of less number of switches when compared to the other familiar topologies. By switching the MOSFETS at the appropriate firing angles, we can obtain the seven level output voltage. MOSFET is preferred because of its fast switching nature. Because of the reduction in the number of switches the initial cost reduces, controlling becomes easier, losses becomes less due to the elimination of the harmonics, overall weight reduces because of the usage of less number of components. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids.

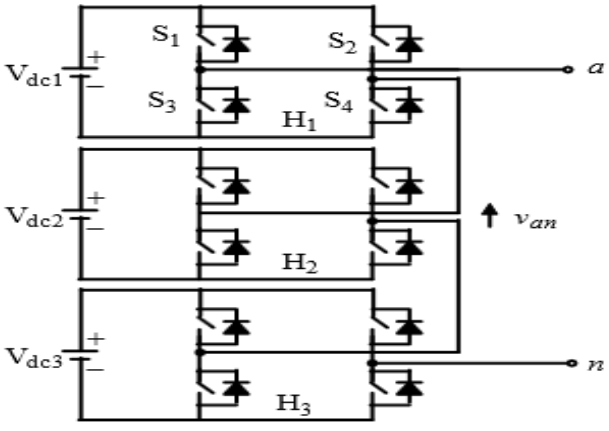

Fig.2 circuit diagram of seven level Proposed Multilevel Inverter

Fig 2 shows a 7 level CMLI by connecting the output of each cell will have three levels +Vdc , 0 and −Vdc that obtained by connecting the dc source to the ac output by different combinations of the four switches S1 , S2 , S3 and S4 . To obtain +Vdc , switches S1 and S4 are turned on, whereas −Vdc can be obtained by turning on switches S2 and S4 . By turning on S1 and S2 or S3 and S4, the output voltage is 0. The output voltage is the sum of the voltage that is generated by each cell.

III. CASCADED MULTILEVEL INVERTER BASED STATCOM

Static VAR compensation by cascading conventional multilevel/ inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/ inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. This improves Power quality Therefore; overall control is simple compared to conventional multilevel inverters.

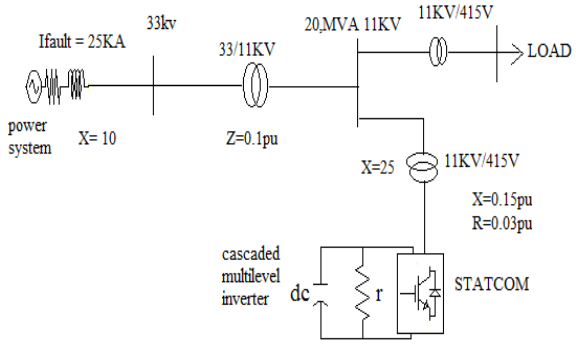

Fig 3 Power System and STATCOM Model

Various var compensation schemes based on this topology are reported. In a three-level inverter and multilevel inverter are connected on either side of the transformer low-voltage winding. The dc-link voltages are maintained by separate converters. In seven-level operation is obtained by using standard multilevel inverters. The dc-link voltage balance between the inverters is affected by the reactive power supplied on the grid.

IV SHE PWM (SELECTIVE HARMONIC ELIMINATION)

There are many popular methods are used to reduce the harmonics in order to get an effective

results. The popular methods for high switching frequency are Sinusoidal PWM and Space Vector PWM. For low switching frequency methods are space vector modulation and selective harmonic elimination. The SPWM technique has disadvantage that it cannot completely eliminate the low order harmonics. Due to this it cause loss and high filter requirement is needed. In Space Vector Modulation technique cannot be applied for unbalanced DC voltages. SHE PWM technique uses many minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to *s*-1 harmonic contents can be removed from the voltage waveform. To keep the number of eliminated harmonics at a constant level, all switching angles must satisfy the condition.

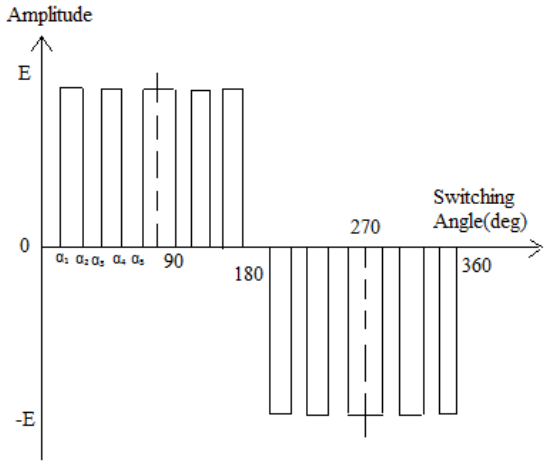

Fig 4 Typical SHE PWM Pattern

A.HARMONIC ELIMINATION THEORY

By applying Fourier series analysis, the output voltage can be obtained. Fourier Series is an infinite sum of trigonometric functions that are economically related

$$F(t) = ao + \sum_{n=1}^{\infty} cn \cos(2\pi nfo + \emptyset n)$$

Where,

N= Integer Multiple

A_o and C_o=Fourier coefficient

$$V(t) = \sum_{n=1,2,5}^{\infty} \frac{4vdc}{n\pi}(V1\cos(n\emptyset 1)) + V2cos(n\emptyset 1) \ldots Vs\cos(n\emptyset 2)$$

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selective harmonic modulation method is proposed, which is called virtual stage PWM An output waveform.

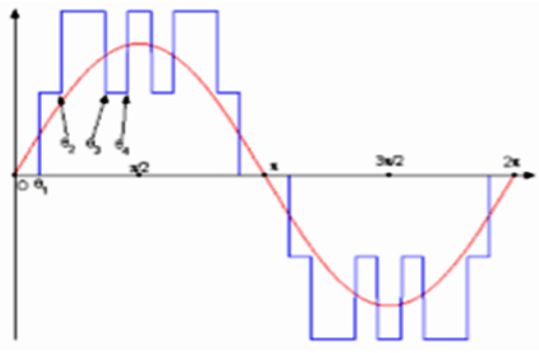

Fig.4.1 Output waveform of virtual stage PWM control

Hence the relation between the fundamental voltage and maximum voltage is given by modulation Index. It is given by m1, is the ratio of fundamental voltage v1 to the maximum voltage.

$$V1max = \frac{4}{\pi} sVdc$$

$$M = \frac{\pi V1}{4SVdc}(3)$$

For an 7- level inverter, there are 4 H-bridges per phase so, s=4 five degrees are available one degree is used to control the magnitude of fundamental voltage and remaining degrees are used to eliminate 5th, 7th, 11th, and 13th order harmonic components.

$$COS(\theta 1) + COS(\theta 2) + .. + COS(\theta s) = 4m1$$
$$COS(5\theta 1) + COS(5\theta 2) + .. + COS(5\theta s) = 0$$
$$COS(7\theta 1) + COS(7\theta 2) + .. + COS(7\theta s) = 0$$

The above equation is a four transcended equations known as Selective Harmonic Elimination.

V. CONTROL STARTERGY

The proposed STATCOM level cascaded inverter connected to a t power system feeding an RL load at conditions (i.e. power factors). The control current controller of the STATCOM propose employed to this work. The operation of the relies on the availability of variable DC voltage should be obtained by various approaches converters are chosen in this work to voltage levels for each H-bridge inverter resultant modulation index due to its operation with small size output *LC* filter an design.

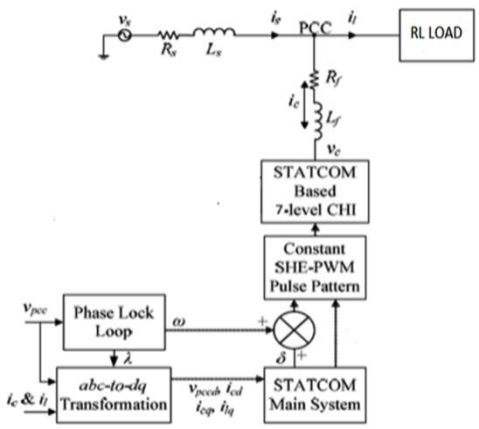

FIG 5.1 STATCOM CONTROL STARGEY

The control block diagram is shown in Fig. 5.1. The unit signals and are generated from the phase-locked loop (PLL) using three-phase supply voltages. The proportional constant that determines the dynamic response of the DC-bus voltage control and K_i is the integration constant that determines the settling time and also the K_d is the derivative of the error representing the trends.

VI. PERFORMANCE EVALUATION

A. Simulation circuit of CMLI for she pwm technique STATCOM

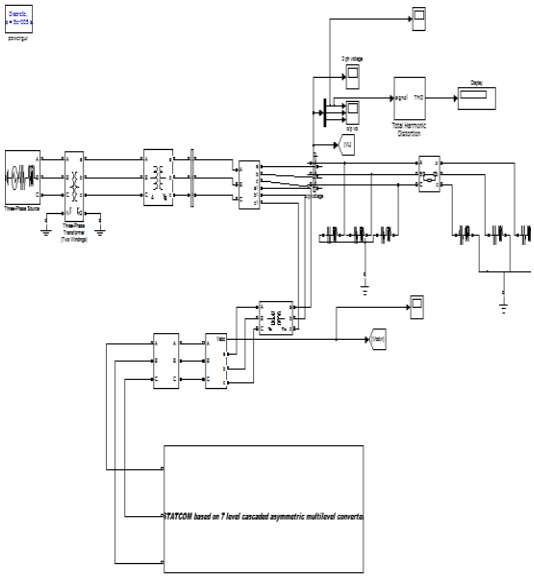

Fig 6.1 shows the model of selective harmonic elimination PWM for the control of cascaded multilevel inverters for STATCOM system.

B.CONTROL SET UP FOR SHE-PWM

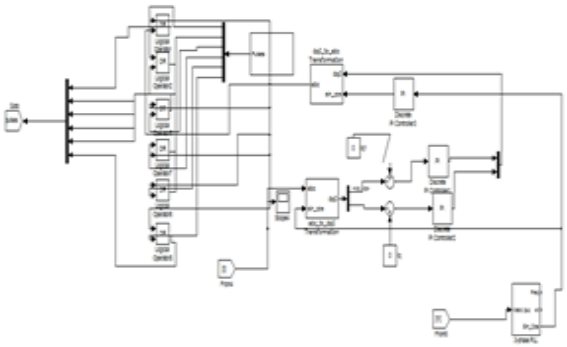

Fig 6.2 CONTROL PARAMETERS OF VARIOUS CONTROLLERS FOR SELECTIVE HARMONIC PWM

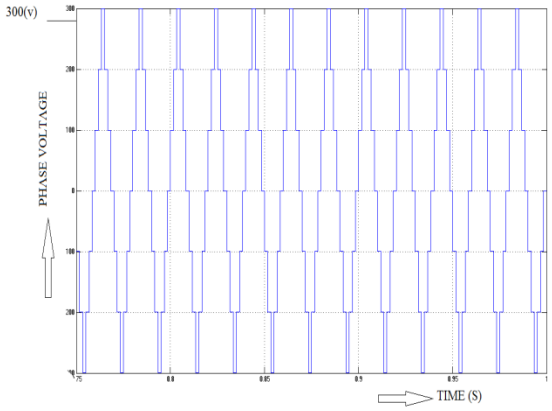

Fig 6.3 OUTPUT OF SEVEN LEVEL INVERTER

C.OUTPUT OF 3 PHASE VOLTAGE

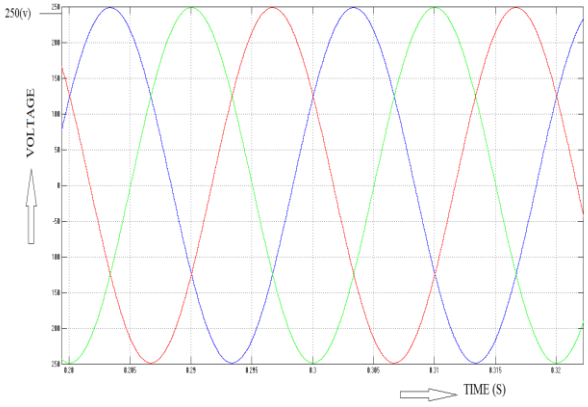

Fig 6.4 RECEVING END LOAD OUTPUT VOLTAGE AND COMPANSTED VOLTAGE

D.COMPENSATION CURRENT FOR STATCOM

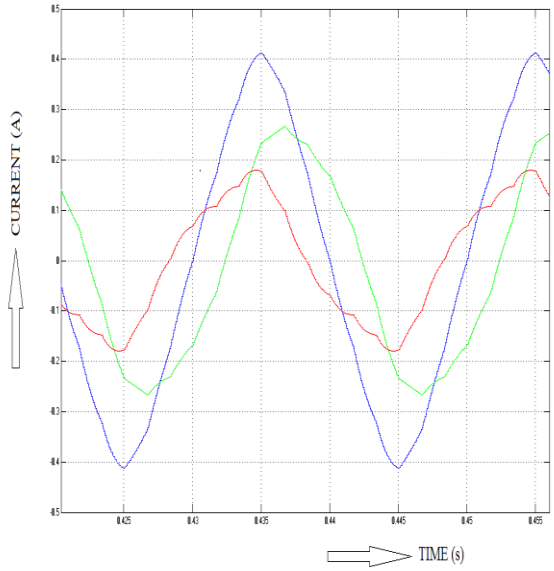

Fig 6.5 WAVEFORM OF STATCOM COMPENSTATION CURRENT OF LOAD SIDE

E. LINE VOLTAGES

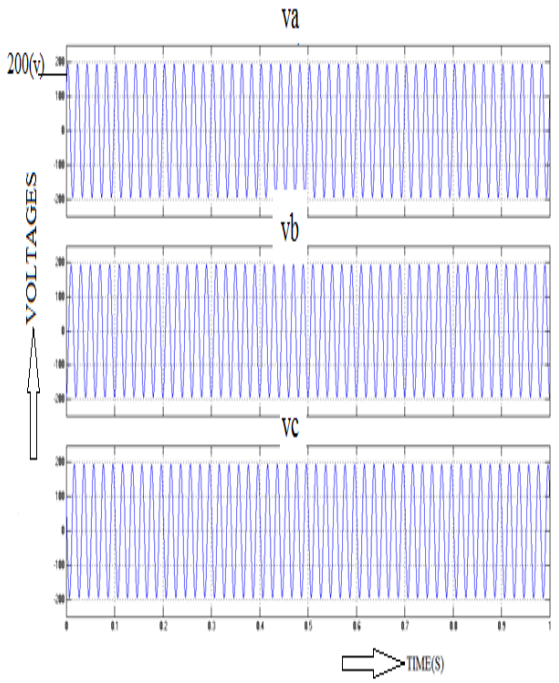

Fig 6.6 LOAD SIDE LINE TO LINE VOLTAGE FOR GRID SIDE

VI. COMPARISON OF SIMULATION RESULTS

HARMONIC ORDER	THD VALU (%) TWO LEVEL INVERTER	THD VALUE(%) USING SHE PWM TECHNIQUE
3	35	0
5	14	0.01
7	12	0.02
13	7	2

FIG 6.1 OUTPUTS COMPARSION TABLE

The calculated values are compared with each other. From the output comparisons Selective harmonic elimination technique gives reduced the lower order harmonics.

VII.CONCLUSION

The simulation of the seven-level multilevel inverter is successfully done using Selective Harmonic Elimination pulse width modulation technique for STATCOM application. The proposed formulation provides an output with wider range of modulation indexes Mi. by making the DC sources variant without affecting the number of harmonics being eliminated. The proposed strategy in the performance of voltage and reactive current compensation at different loading conditions for STATCOM. From the simulation results we calculated THD value and compared the THD value of multilevel inverter with ordinary PWM technique and SHE PWM technique. Thus Individual THD value is reduced using SHE-PWM Technique. The performance is verified by using RL load and verified by MATLAB/SIMULINK software.

REFERENCES

1. EbrahimBabaei, 2008, A Cascade Multilevel Converter Topology With Reduced Number of Switches IEEE Transactions on power electronics,Vol. 23, No.6.

2. J. Rodríguez, J. S. Lai, and F. Z. Peng, Multilevel inverters: A survey of topologies, controls, and applications, IEEE Transaction on Industrial electronics, vol. 49, no. 4, pp. 724–738, Aug. 2002 .

3. Mohan N, Undeland T. M, and Robbins W.P. 2003, Power Electronics: converters, applications and design‖, Third Edition.John Wiley and sons.

4. Selective Harmonics Elimination of PWM cascaded multilevel inverter ANIKET ANAND1, K.P.SINGH2 Department of Electrical EngineeringMadan Mohan Malaviya Engineering College Gorakhpur-273010, India

5. Selective harmonics elimination pwm with self-balancing dc-link capacitors in five-level inverter K. Imarazene1, H. Chekireb2 And E.M. Berkouk2

6. new approach to solving the harmonic elimination equations for a multilevel converte, in Proc. IEEEIndustry Applications Soc. Annu. Meeting, Salt Lake City, UT, pp. 640-645, Oct.12-16, 2003.

7. BurakOzpineci, Leon M. Tolbert, John N. Chiasson, Harmonic Optimization of Multilevel Converters Using Genetic Algorithm, IEEE Power Electronics Letters, vol. 3, no. 3, pp.92-95, September 2005.

8. C. Woodford and C. Phillips, Numerical Methods with Worked Example, CHAPMAN & HALL, pp. 45-57, First edition 1997

9. S. R. Bowes and S. Grewal, Simplified harmonic elimination PWM control strategy Proc. Inst. Elect. Eng.—Electron. Lett., vol. 34, no. 4, pp. 325–326, Feb. 19, 1998.

10. V.G. Agelidis, A. Balouktsis and M. S.A. Dahidah, "A five-level symmetrically defined selective harmonic elimination PWM strategy: analysis and experimental validation," *IEEE Trans. on Power Electronics*, vol. 23, no. 1, January 2008, pp. 19-26.

11. M.S.A. Dahidah and V.G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula", *IEEE Trans. Power Electron*., vol. 23, no. 4, pp. 1620-1630, Jul. 2008.

12. Selective harmonics elimination pwm with self-balancing dc-link capacitors in five-level inverter K. Imarazene1, H. Chekireb2 And E.M. Berkouk2