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An Efficient Design of Optimized Low Power Dual Mode Logic Circuits Using VLSI Technology

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Abstract - This project represents a dual mode logic circuit for low power applications.Now a day's power consumption is the major role in chip design .If the area ofthe chip is reduced, the power consumption and the delays are increased due tosome effects like, cross talk, process variation and channel effects of MOSdevices. The CMOS logics are most used in logic design. But it has someDisadvantages related with power consumption. So we can go to the dual modelogic. The proposed logic is operated between static mode and dynamic mode.In normal CMOS logic it requires different type of circuits for static anddynamic mode. But this proposed logic operates in both modes in a singlecircuit .The 4 bit carry look ahead adder is designed by dual mode logic in thisproject. It was designed in sub threshold region and various process technologieslike 90nm, 70nm, 50nm and 32nm.The proposed CLA adder is compiled asdigital circuit, as well analog circuit and power consumption, delay & area weremeasured. It has been compared with existing static CMOS logic and dynamic CMOS logic with various process technologies.

Keywords— Micro wind,CMOS,Dual Mode Logic,CLA Adder,VLSI Technology.

I. INTRODUCTION

The digital circuits are the most important blocks in Integrated circuits. For compact digital circuits and ICs ultra low power circuits are required [1]. So the main option for the digital circuit is CMOS Devices. In CMOS Digital circuits there are many types of logic families are available. The most used logics are static CMOS and dynamic CMOS. But these are havingdifferent constructions. The static CMOS circuits are constructed by both NMOS and PMOS devices.The logical operation evaluated by the combination of input values. The dynamic CMOS circuits are constructed by only pull down network. The keeper and header transistors are connected with clock signal [2].But both the logics are having some disadvantages like charge sharing, transistor count, transistor ratio, clock rate etc and these are the different physical structures [1]. The proposed Dual mode logic is operates between static and dynamic modes of operation with a single circuit [3]. The clock signal is a mode selecting signal for this logic.It can be a continuous clock signal or a fixed pulse signal depends on type of operating mode.

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II. DUAL MODE LOGIC

The basic DML gate is constructed by the standard CMOS gate. These standard CMOS gates having both pull up network and pull down network. It should have one or more inputs and one output. This output connected to the switching element. The total block is a DML gate. The switching element chooses the operating mode by voltage signal or clock signal. The block diagram of basic DML gate is shown in Fig.1. Normally DML circuits are constructed by twotopologies. The switching element type and its place decide the type of topology. These switching elements are connected to control signal.

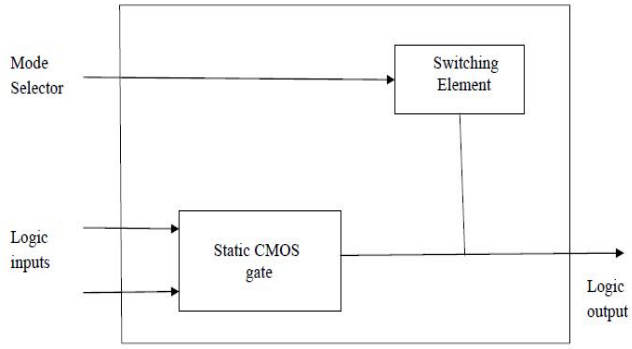

Fig.1 Block diagram of basic DML gate.

It depends on the type of switching element. The following are the two types of DML topologies.

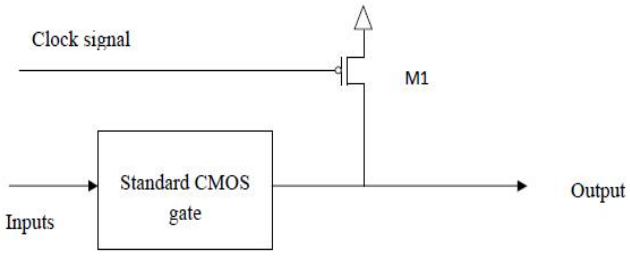

Fig.2 Type A Topology

In type A topology the standard CMOS gate is connected to the pull up(PMOS) transistor M1, whose gate is connected to a global clock signal, source is connected to VDD and drain is connected to the output function of the standard CMOS gate [3], [4].Fig.2 shows the block diagram of type A topology. Here the clock signal is operates as a mode selecting signal. In type B topology the standard CMOS gate is connected to the pull down (NMOS)transistor M1, whose gate is connected to a

global clock signal, source is connected to groundand drain is connected to the output function of the standard CMOS gate.Fig.3 shows theblock diagram of type B topology. Here the clock signal is operates as a mode selectingsignal. The clock signal isassigned to asymmetric clock signal at the time of dynamic operation.

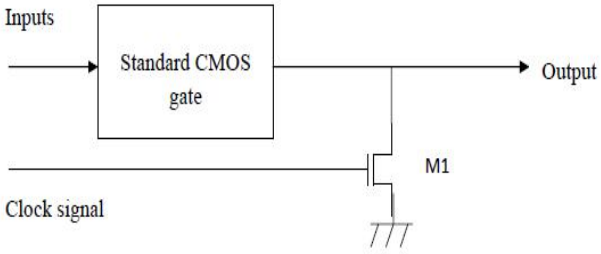

Fig.3 Type B Topology

III. DESIGN OF 4-BIT DML CLA ADDER

The proposed 4 bit carry look ahead adder is designed by dual mode logic. The Four bit CLA adder block is shown in Fig.4.The proposed CLA adders is constructed by both pull up and pull down network, and the switching element is attached at the end of the output. It has two output lines in each bit, suchas sum and carry. For 4 bit operation it has four blocks and each block contains PMOS and NMOS transistors [8], [9]. The construction is made by the following expressions,

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

The outputs sum and carry can be called expressed as

$S_i = Pi \oplus Ci$

$C_{i+1} = G_i + P_i C_i$

Where $G_i$is a carry generate and Pi is called a carry propagate. The Boolean function of the carry outputs of each stage are,

C_0=input carry

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

If there is no input carry, then C0 becomes 0 and the last term in each expression forcarry will be eliminated. Although these expressions become very lengthy as the bitsignificance increases, each expression is only three logic levels deep, so the delay in formingthe carry is constant irrespective of bit position.

Each sum output requires two exclusive-OR functions. The output of the firstexclusive-OR generates the Pi variable, and the AND operation generates the Gi variable. Thecarries are propagated through the carry look ahead generator and applied as inputs to thesecond exclusive-OR function. All output carries are generated after a delay through twolevels of gates. Thus, outputs S1 through S3 have equal propagation delay times.

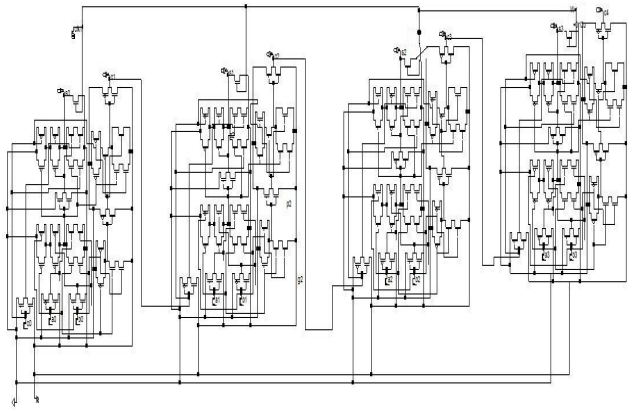

Fig 4. 4 bit CLA adder using dual mode logic

A. Operation

Switching the DML CLA Adder between the two functional modes, static and dynamic, is performed by applying either a constant voltage or a dynamic clock signal at the mode selection input of the switching element. When static functional mode is selected an appropriate constant voltage (high or low as required by static gate topology) is applied to the mode selection input of the switching element [5]. For topology A, high voltage and for topology B, low voltage (zero) is applied. The applied constant voltage causes the switching element to disconnect the static gate output from the constant voltage applied, thus enabling static mode of operation. During dynamic mode of operation, the switching element input is a dynamic clock signal which has pre-charge and evaluate phases, which will periodically connect the static gate output to the constant voltage level, thus enabling dynamic mode of operation [6]. During pre-charge phase the output charged to VDD and during evaluation phase the expected output comes dependent on input combination.The evaluation is performed with the parallel transistors and, therefore, it is faster. The stacked transistors will be sized to minimal widths to reduce intrinsic capacitances, increasing dynamic operation performance over reduced static operation performance [7]. This sizing strategy also results in reduced energy dissipation, as compared to conventional static CMOS gates. The pre charge transistor is also minimum sized to decrease leakage currents during static operation and evaluation.

IV. SIMULATION ENVIRONMENT

A. Transistor parameters

The proposed DML CLA adder is designed by both NMOS and PMOS transistors. The VDD is taken as minimum voltage according to its process technology and also channel length of the transistor was taken as minimum like 50nm, 70nm, and 90nm.Total design consists of 80 NMOS transistors and 76PMOS transistors. The proposed circuit was designed by topology B.

B. Device model

In this project we use simple MOS level 1 model for NMOS and PMOSdevices. For theevaluation of the current Ids between the drain and the source as a function of Vd,Vg, and Vshere use the old but nevertheless simple level 1 described below [9], [10]. The level 1 device model can calculate the devicecurrents from the following equations,

ICUTOFF = 0

IOHMIC=K'(W/Leff)([VGS– VTH] – (VDS/2))VDS

ISAT = (K'/2)(W/Leff)(VGS – VTH)

K' = μCOX

Where, K' – Trans conductance parameter, μ - Channel mobility, COX – Gate oxide capacitance, Leff – Effective channel length, W - Channel width, VTH – Threshold voltage, VGS – Gate-source voltage, VDS - Drain-source voltage

C. Design rules

The proposed CLA Adder is designed based on lambda rules. In general, design rules and layout methodology based on the concept of λ provide a process and feature size independent way of setting out mask dimensions to scale [10]. All paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

D. Process Variation Model

One important challenge in NANO CMOS technology is process variation. The fabrication of millions of MOS devices at NANO scale induces a spreading in switching parameters in the same IC. The most important parameter affected by process variability is the threshold voltage, the carrier mobility and the effective channel length. Variations are handles in this project, using random values in a Gaussian distribution, which is expressed by the following equation

$$e^{(x-m)/2\sigma}$$

Where,

- Probability density of the random variable, x – Variance σ – Deviation and m – Mean value.

E. Tool used

The proposed DML CLA Adder is designed by MICROWIND 3.1 software. It isone of the efficient back end tools to design analog circuits at layout level. This softwaredesigned by Mr. EtienneSicard from France. The MICROWIND program allows designing and simulating an integrated atphysical description level. The package contains a library common logic and analog ICs toview and simulate.

V. COMPARISION RESULTS

The proposed DML CLA Adder was simulated with 90nm, 70nm, 50nm, and 32nm process technologies. The same CLA adder was constructed by static and dynamic CMOS logics and the simulation results are compared with the proposed DML results. Fig 5 shows the output of DML CLA Adder when operate as a static mode in 32nm process technology.

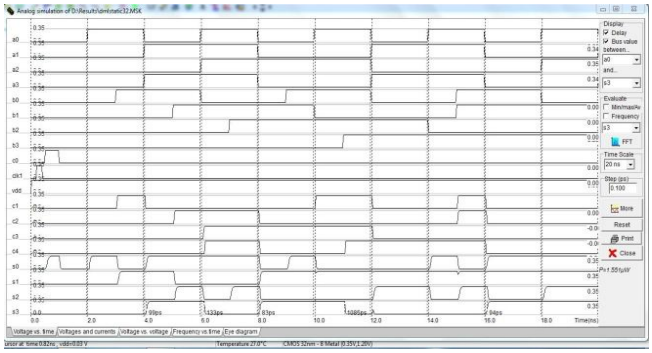

Fig.5.DML CLA Adder output – static mode

The output of proposed DML CLA Adder at dynamic mode using 32nm process technology is shown in Fig.6.

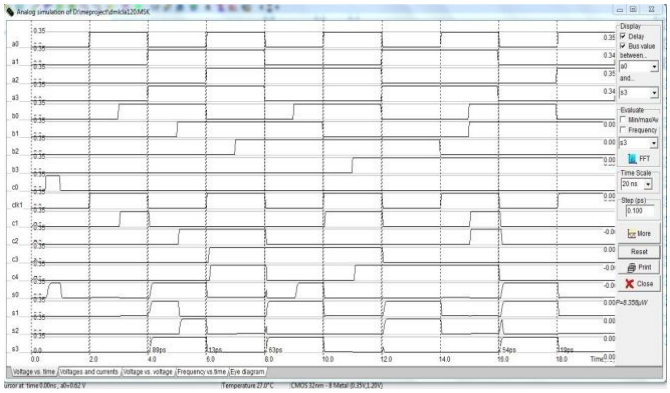

Fig.6.DML CLA Adder output – Dynamic mode

A. Power dissipation

In complementary inverter based circuits we may proceed by first recognizing that the very short current pulses which flow when circuits of this type are switching between states are generally negligible in comparison with charge and discharge currents of circuit capacitances. The proposed CLA adder gives two different types of power dissipation dependent upon the mode of operation .It gives low power dissipation in static mode and moderate power dissipation in dynamic mode. It consumes 1.551μw in 32nm technology. It is very low compared with normal static CMOS circuits. Fig.7. shows the graph of power consumption for various technologies.The

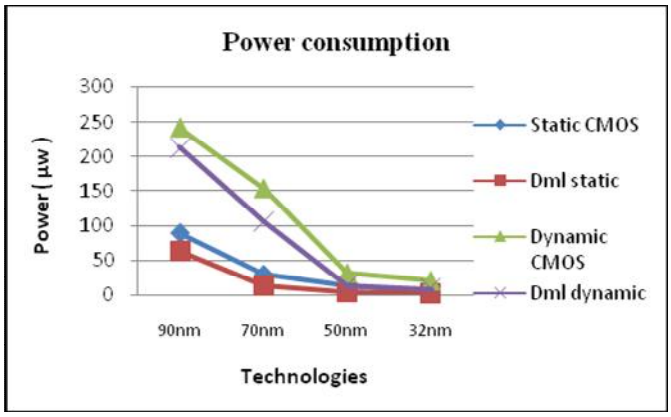

Fig.7 power consumption chart.

Table2 shows the comparison of power consumption of proposed DML CLA Adder with conventional static CMOS and dynamic CMOS CLA Adder at various process technologies. The power consumption is measured for 20ns time scale with the 100ps step samples.

B. .Delay

The speed of the proposed CLA is compared with the static CMOS CLA circuit. It gives two different level of operation. In dynamic mode of operation it achieves efficient speed. That is the delay is reduced to 47.6ps in 32nm technology.The proposed design is simulated in various technologies like, 90nm, 70nm, 50nm, and 32nm. Out of these results these results 32nm technology got good speed of operation and also the static mode of operation has good speed Compared with normal static CMOS logic.

Table 2 Comparison of Power Consumption.

Technologies	Power consumption (µw)			
	Static CMOS	DML-Static mode	Dynamic CMOS	DML-Dynamic mode
90 nm	88.972	63.362	241	213
70 nm	29.756	12.594	153	105
50 nm	13.650	2.606	31.671	13.65
32 nm	4.319	1.551	20.535	8.358

Table 3 Comparison of Average time delay

Technologies	Average time Delay (ps)			
	Static CMOS	DML-Static mode	Dynamic CMOS	DML-Dynamic mode
90 nm	58.5	251.4	91.25	44.5
70 nm	60	250.8	77.33	37.33
50 nm	96.5	304.4	83.5	46.5
32 nm	80	298.8	92	47.6

It gives 47.6ps ofaverage delay but the dynamic CMOS CLA adder was taken as 80ps.it also simulated with various technologies. The operating frequency of this design is calculated from minimal operating period T. It was determined from the following equation.

Where t_{HL} is transition time from high to low and t_{LH} is transition time from low to high. Fig 8 shows the graph of different time delays of the proposed adder with various technologies.

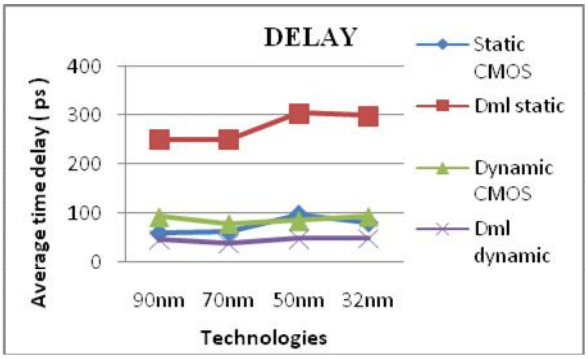

Fig.8. Graph of delay with various technologies

The table 3 shows the comparison of Average time delay of proposed DML CLA Adder with various process technologies.

C. Area

The proposed CLA adder is designed in various nanometer technologies to reduce the area of the layout.These technologies are describes the channel length of the MOS devices. For each technology, various design rules and value of λ were chosen. Dependent on the technologies area of the

Chip, are varied. One of the main objectives of the minimum nm technology is to reduce the area of the chip.Fig.9 shows the graph of area of the chip for various technologies.

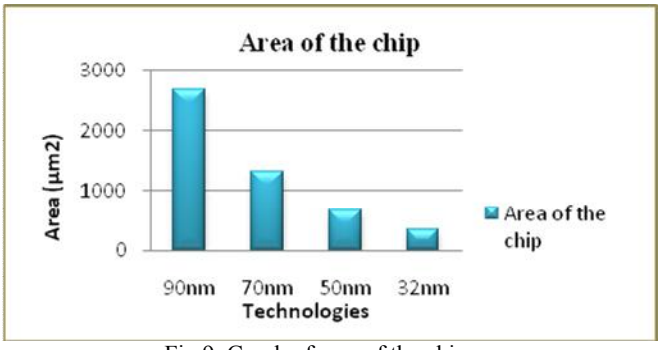

Fig.9. Graph of area of the chip

The proposed DML CLA adder is designed in chip level .

The 32 nm technology chip gives the reduced area of 427.7µm^2.

VI. CONCLUSION

The proposed dual mode logic circuit is evaluated using 4 bit carry look ahead adder. It is the efficient logic family than conventional CMOS family. It was tested under various technologies like 32nm, 50nm, 70nm, 90nm and results were compared with conventional static and dynamic CMOS logic circuits.The proposed design reduces the power consumption and time delay and also a single circuit operates as static circuit and dynamic circuit without any physical modification. The layout size was reduced when this circuit designed from 90nm to 32nm process technology. This dual mode logic gives efficient result at 32nm process technology with low power consumption and minimum average time delay.

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