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A Survey on Distributed Packet Buffer for High bandwidth Routers

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Abstract— Distributed packet buffer support multiple queues and provide large capacity and short response time. To build the packet buffers based on a hybrid SRAM /DRAM they introduce minimum overhead problems to avoid these type of causes throughput and storage capacity of the packet buffer are increased. Previous algorithms are shows a little effects in parallel DRAMs. In this paper aims to increase the efficiency of the router at the high bandwidth usage paths in network using parallel Buffering techniques.

Keywords: SRAM/ DRAM, Parallel Buffer, Hybrid DRAM, Router memory

I. INTRODUCTION

Networking is the process of supplying data and information by linking the group of networks using hardware's. A hardware that are switches, hubs gateways, access points, network interface cards, networking cables, etc. that are more specific in networking. The tools that are required for communication and data processing in the network are all computer peripherals, computers and interface cards.

The growth of internet usage demands the increase in communication link bandwidth. But the routers are still an open issue to sustain the growth of internet usage. To avoid these demands packet switching and buffering techniques are used. Packet buffers are used to support large capacity, multiple queues while providing short response time.

The router that should capable of buffering RTT*R (Round Trip Time * Line Rate). The efficiency of the router are determined based on the small expense and a small loss in throughput but an individual TCP flow for input/output capacity ratio at network link are to determine the buffer size. Current router manufacturers are still using large buffers. A CISCO CRS-1 modular service card with 40Gbps line rate, use 2GB packet buffer memory per line card [1].

In order to support QOS [Quality of service] thousands of queues are maintained by a packet buffer. For example juniper E- series router maintains 64000 queues, that dynamically manages the shared memory egress line modules to provide a good balance between sharing the memory among queue and protecting the individual queues.

A packet buffer should be capable of sustaining ingress and egress. But the increase of line rate in current technology's SRAM/ DRAM alone cannot satisfy the packet buffer requirements. So the researcher suggests hybrid SRAM / DRAM architectures to buffer the data.

II. LITERATURE REVIEW

To avoid the loss of packets in data transfer over the network Dong Lin [2] proposed the architecture with SRAM / DRAM. It combines the merits of two previously used packet buffer architectures [4][5]. The result of these combinations SRAM occupancies has been reduced, but some problems might occur in DRAM. So the researcher moves on to parallel DRAM with the use of Random Round Robin (RRR) Memory Management Algorithm (MMA). The implementation uses the centralized queue table for packet buffer. A packet buffer can track the status of individual logical queues and the memory address of physical queues. An increase of logical queues and overall throughput a bottleneck problem caused in the entire system. To avoid this bottleneck, a hierarchical structure used to reduce the number of physical queues lead to smaller queue table.

Hybrid SRAM / DRAM architecture with one DRAM and two smaller SRAMs employed. The two SRAMs hold far head and tail for all the queues. The idea which are used for memory management algorithm, that temporarily holds O(b) of data of each queue for both ingress and egress of SRAMs. To avoid the implementation issues FIFO queues are used. The FIFO queue accumulate b-size amount of data that transferred to DRAM through single write operation.

To avoid the consistency problem pipelined query and small fully indexed table to store all the recent updates in the datagram are used. The depth of head and tail FIFOs and index table are relay on Round Trip Time of a query. Finally parallel DRAMs are used. The larger SRAM provide high time complexity in memory management.

D.Krishnakumarreddy et al [3] suggests hybrid SRAM/ DRAM architecture with a single DRAM, interleaved DRAMS or parallel DRAMS sandwiched between SRAMs. The previous packet buffer architecture and present scalable hierarchical packet buffer architecture are reviewed. They can use traffic- aware approach to provide different services for the different data streams. These proposed architectures reduce the size of SRAM by 95% and no change in delay. In contrast, the line-rate increases by 100% every 18 months the

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DRAM will fall to satisfying the requirements of high speed buffers.

To keep the DRAM modules busy, we need to transfer the minimum size chunk. The current chunk size of DRAM ranges 64 to 320 bytes. The high latency DRAM product (DDR3) has 320bytes chunk. To avoid the load balancing problem per-destination and per- packet load balancing in the packet buffer architecture are adopted. But the problem occurred once the buffer is filled with packets only the ingress of data to the router.

D.Lin et al [4] designed a packet buffer for high-bandwidth routers and switches with the use of hybrid SRAM/ DRAM for combining the SRAM / DRAM to supports multiple queues, large capacity and short response time. A scalable packet buffer using independent buffer subsystem helped to find the workload among multiple buffer system without blocking.

This design dispenses with head and tail cache and keeps only tiny distributed front-buffer inside each subsystem. Each flow was mapped with one buffer. So the physical queues usages are reduced and the size of SRAM also reduced significantly.

D.Lin et al [5] designed a packet buffer with the use of Random Round Robin technique they present novel packet buffer architecture to reduce the SRAM size requirements by (k-1)/2k, where k is DRAMs that working parallel. They use per – queue Random Robin and fast batch-load scheme. Problems occurred in capacity, short response time and multiple queues while using the Single SRAM /DRAM. So they move on to hybrid SRAM / DRAM architecture with single DRAM and parallel DRAMs. To introduce these methods the typical memory access time of DRAM increased too large.

To organize the memories they suggest two ways that are independent address bus organization and shared address bus organization. While using independent address bus fundamental access problems have been reduced and DRAMs are capable of accommodating b-size of chunks, for using shared address bus the memory access is always at the same address and the size of DRAM memory chunk become kb.

D.Lin et al [6] proposed two stage fair queue budget round robin techniques to avoid fair allocation of network resources in high bandwidth-delay-product networks and traditional end-to- end network protocols. Fair-queuing (FQ) algorithm are used to overcome the drawback of dropped packets in intermediate routers. But FQ algorithm is more difficult to implement in large scale because of its high time-complexity or greater rely on the multiple queuing structure and sometime it cause a delay of DRAM. To avoid this delay a new algorithm called Budget Round Robin are introduced. This is useful for high speed internet connections. In addition, dynamic quantum adjustment is used in architecture to increase the memory utilization.

For implementation memory utilization and quondam adjustment in Budget Round Robin (BRR) algorithms are used. The BRR algorithm is not only for allocation of bandwidth that is used to reserve the storage for all active connections. To avoid memory allocation problem dynamic buffer allocation are used. It allows the buffer to share the blocks for provide higher efficiency. To merge two DRAM blocks into one block is difficult in practice. To overcome the difficulty BRR was used instead of adjusting DRAMs.

G. ManjunathReddy et al[7] developed some of the theorems for high bandwidth switches and routers. These theorems are used to find the buffer size, the available memory size and optical data storage. what all the reasons a router have a buffer, and also they can use semi parallel hybrid SRAM / DRAM packet buffer architecture to buffer the data's from the communication links in optical buffers.

High speed Internet routers and switches require the fast packet buffer to hold packets during times of congestion. These buffers usually use a memory hierarchy that consists of expensive, fast SRAM and cheap but slow DRAM to meet both, speed and capacity requirements. A challenge in building these packet buffers is to provide a deterministic bandwidth guarantee under any traffic condition. Novel hybrid packet buffer architecture with parallel DRAMs is used. This approach reduces the amount of required SRAM compared to state-of-the-art architectures significantly, e.g., the tail SRAM by 47% for a 100Gbps line card using DDR3 SDRAM. Optical buffer architecture also applies packet aggregation and thereby minimizes the required DRAM and SRAM bandwidth and eliminates fragmentation. We are currently implementing the architecture on an FPGA and provide first results

K. Ascherya et al[8] described 64 byte cell sized packet buffer for high bandwidth routers. They can use FIFO (First In First Out) queue technique to buffer the data from the switches. An write and read operation are performed one after another. The performance of the ingress in FIFO queue is measured with key size K. If a data with size K is transferred to DRAM a single write operation was performed if suppose 2 write operations of K size performed on a queue means an overflow of data may occur.

In 64 bytes DRAM the chunk size is determined by two factors that are bandwidth and typical memory access time. The only drawback in the working nature of the architecture was they gave only the first 64 bytes of data that are arriving into a queue. Then the data's are stored in SRAM infinitely. But the current available DRAM is around 64 to 320 Bytes of size. When the first DRAM receives all the data of 64 bytes an unbalance traffic allocation was created among the DRAMs. To avoid these long-term output balance per-queue round robin scheme was implemented. If the heads of the current active queues in the output may allocate to a particular DRAM means which leads a bottleneck of the entire system. But the architecture proposes low time complexity with short access delay.

Kalyan varadhan et al [9] designed a new architecture of memory to reduce the system overhead in terms of size of SRAM. Random Round Robin technique used to dispatch b-sized chunks between the DRAMs. An issue over the design are minimizing the transparency of an individual packet buffer

and designing the scalable packet buffer by means of autonomous buffer subsystem. So to avoid the unbalancing they use a fixed size simulation.

To minimize the transparency of an individual packet buffer two kinds of patterns of traffic such as uniform and unbalanced traffic was created. A uniform traffic alters the intensity of traffic. In a uniform design the cache of tail is unfilled, that consistently assigns cells between each and every one queues that generating a smaller amount of dispatchable chunks.

S.Iyer et al [10] designed a router with SRAM / DRAM. For designing a higher capacity router is challenging to design buffer because the buffer size and speed are increased linearly with line- rate. If the line rate will increase the line cards (Routers) are connect more lines and the buffer also larger. To avoid linecard increase ratio two goals are described, that are arriving packets are written to the DRAM before the SRAM overflow and departing packets are in SRAM when their turn to leave.

To reduce the b-size chunks in the SRAM a new buffering algorithm are used that is "ping-pong" buffering. Here the memory is divided into two equal groups and one block on a group. For each routing process the blocks are read as before the data through into the block. The block size b=RT. Once the block size is reduced one of the groups will become full, the buffer cannot be filled and half of the memory will be used. By saving the memory density and bandwidth the "65 byte problem" was arises, usually 64 byte of cells is used in switch fabric but the minimum length is increased in the IP datagram. To avoid 65 byte problem the data are filled in SRAM are partially. In an implementation of packet buffer that run 2R and there will not cause the external memory problem.

Sandeep M Gundale [11] proposed a design for packet buffer for high-bandwidth switches and routers. There are two main topics are described to make a design succeeded that are minimize the overhead of individual packet buffer and combine the SRAM and DRAM hierarchical buffer design.

To avid overhead of individual packet buffer Hybrid SRAM and Parallel DRAM methods are used. With the use Parallel DRAM usage of SRAM has been compressed. They can use Random Round Robin algorithm for Memory Allocation. The approach which are mainly implemented here are "Traffic-Aware", that aims to provide different services in the network. An interrupted DRAM was designed to fix the scaling limitations in SRAM and to increase the SRAM size. With the use interrupted DRAM and increased SRAM size methodology bandwidth and storage capacity may increased and many DRAMs can working parallel. But the issue over the design was centralized queue table. With the increase of logical queues a centralized queue table cause blockage of the entire system.

III. CONCLUSION

From the consideration of all the above points we conclude that the loss of packets in data transfer over the network still an open issue. In this paper, we suggest parallel buffer and packet grouping algorithms to reduce the delay in the SRAM. Our analysis shows that previous algorithms make very little effects in exploring the advantages of parallel DRAM leading to the requirements of large size SRAM and time complexity in memory management. Distributed packet buffer architecture provides low time complexity, short access delay, and upper bounded drop rate.

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